ABSTRACT

A semiconductor memory device includes a plurality of memory cells each capable of storing and programming N-level data; a reference cell storing a reference level used when reading a data level stored in the memory cells; a counter circuit counting number of times of reading of the reference cell; a check means for determining whether the reference level stored in the reference cell is within a preset range when the number of times of reading that is counted reaches a specified value; and a correction means for, if the check means determines that the reference level is out of the range, correcting the reference level to fall within the range in accordance with a master reference cell. With this constitution, it is possible to provide the semiconductor memory device capable of efficiently correcting the state of the reference cell, preventing the deterioration of the reference cell due to disturbance or the like, and highly accurately maintaining the level of the reference cell.

Reference Drawing: Fig. 1